CLAIMS

What is claimed is:

1. A computer implemented method for determining timing delay for a circuit in an integrated circuit, said method comprising the steps of:

determining a resistive-capacitive ("RC") network between a driving point and a receiving point, said circuit driving said RC network at said driving point;

storing a circuit characterization model for said circuit, said circuit characterization model depicting relationships among input signal slew rate, load capacitance, current at said driving point and voltage at said driving point for said circuit;

determining a plurality of effective driving currents for said circuit at said driving point based on said circuit characterization model; and

determining timing delay parameters from said effective driving currents.

2. The method as set forth in claim 1, wherein the step of determining a plurality of effective driving currents comprises the steps of:

selecting an initial drive current;

determining a drive voltage, corresponding to said drive current, by simulating the drive, at said driving point, of said RC network with said initial drive current;

determining an effective capacitance as a load for said circuit;

determining a new drive current for said circuit from said drive voltage and said effective capacitance; and

repeating the steps of determining a drive voltage and determining an effective capacitance for said plurality of drive currents.

3. The method as set forth in claim 1, wherein the step of determining timing delay parameters from said effective driving currents comprises the steps of:

determining a voltage at said driving point from an impedance of said RC network and said driving currents;

determining a voltage at said receiving point from a transfer function of said RC network; and

determining timing parameters for RC network propagation delay from said voltage at said driving point and said voltage at said receiving point.

4. The method as set forth in claim 1, wherein the step of determining timing delay parameters from said effective driving currents comprises the steps of:

receiving an input voltage to said circuit;

determining a voltage at said driving point from an impedance of said RC network and said driving currents; and

determining timing parameters for driving instance delay of said circuit from said input voltage to said voltage at said driving point.

5. The method as set forth in claim 1, further comprising the steps of:

selecting a plurality of time instances corresponding to a plurality of output voltages to said circuit; and

determining a plurality of effective driving currents for said circuit for each of said time instances.

6. The method as set forth in claim 2, wherein the step of determining an effective capacitance comprises the step of determining said effective capacitance based on charging and discharging of said RC network from said drive current.

7. The method as set forth in claim 2, wherein the step of determining a new drive current for said circuit from said drive voltage and said effective capacitance comprises the steps of:

selecting an input signal slew rate for simulation of an input signal to said circuit; and

accessing said circuit characterization model to extract a drive current based on said drive voltage, effective capacitance, and said input signal slew rate selected.

8. The method as set forth in claim 1, wherein:

said integrated circuit comprises at least one standard cell;

said circuit comprises a gate level circuit implemented on said standard cell; and

said RC network comprises an interconnect network on said integrated circuit for coupling said driving point to said receiving point.

9. The method as set forth in claim 1, further comprising the steps of:

selecting, from one of said plurality of drive currents, a drive current with the largest value as a peak current; and

calculating peak power from said peak current.

10. A method for characterizing a circuit for determining a timing delay, said method comprising the step of:

determining a resistive-capacitive ("RC") network between a driving point and a receiving point, said circuit driving said RC network at said driving point;

selecting a plurality of time instances for analysis of said circuit;

determining a load capacitance for each of said time instances, said load capacitance specifying a capacitance from said driving point of said circuit;

determining operation of said circuit at a new time instance based on said load capacitance of a previous time instance; and

determining timing delay parameters based on operation of said circuit and response to said RC network at said time instances.

11. The method as set forth in claim 10, wherein the step of determining operation of said circuit at a new time instance based on said load capacitance of a previous time instance comprises the steps of:

selecting an initial drive current;

determining a drive voltage, corresponding to said drive current, by simulating the drive, at said driving point, of said RC network with said initial drive current;

determining a new drive current for said circuit from said drive voltage and said load capacitance; and

repeating the steps of determining a drive voltage from said load capacitance for said drive currents.

12. The method as set forth in claim 11, wherein the step of determining a new drive current for said circuit from said drive voltage and said load capacitance comprises the steps of:

storing a circuit characterization model for said circuit, said circuit characterization model depicting relationships among input signal slew rate, load capacitance, drive current and drive voltage for said circuit; and

selecting an input signal slew rate for simulation of an input signal to said circuit; and

accessing said circuit characterization model to extract a drive current based on said drive voltage, effective capacitance, and said input signal slew rate selected.

13. A computer readable medium, comprising a plurality of instructions, which when executed by a computer, causes the computer to determine timing delays for a circuit in an integrated circuit, said instructions for:

determining a resistive-capacitive ("RC") network between a driving point and a receiving point, said circuit driving said RC network at said driving point;

storing a circuit characterization model for said circuit, said circuit characterization model depicting relationships among input signal slew rate, load capacitance, current at said driving point and voltage at said driving point for said circuit;

determining a plurality of effective driving currents for said circuit at said driving point based on said circuit characterization model; and

determining timing delay parameters from said effective driving currents.

14. The computer readable medium as set forth in claim 13, the instructions for determining a plurality of effective driving currents comprises instructions for:

selecting an initial drive current;

determining a drive voltage, corresponding to said drive current, by simulating the drive, at said driving point, of said RC network with said initial drive current;

determining an effective capacitance as a load for said circuit;

determining a new drive current for said circuit from said drive voltage and said effective capacitance; and

repeating the steps of determining a drive voltage and determining an effective capacitance for said plurality of drive currents.

15. The computer readable medium as set forth in claim 13, wherein instructions for determining timing delay parameters from said effective driving currents comprises the steps of:

determining a voltage at said driving point from an impedance of said RC network and said driving currents;

determining a voltage at said receiving point from a transfer function of said RC network; and

determining timing parameters for RC network propagation delay from said voltage at said driving point and said voltage at said receiving point.

16. The computer readable medium as set forth in claim 13, wherein instructions for determining timing delay parameters from said effective driving currents comprises instructions for:

receiving an input voltage to said circuit;

determining a voltage at said driving point from an impedance of said RC network and said driving currents; and

determining timing parameters for driving instance delay of said circuit from said input voltage to said voltage at said driving point.

17. The computer readable medium as set forth in claim 13, further comprising instructions for:

selecting a plurality of time instances corresponding to a plurality of output voltages to said circuit; and

determining a plurality of effective driving currents for said circuit for each of said time instances.

18. The computer readable medium as set forth in claim 14, wherein the instructions for determining an effective capacitance comprises instructions for determining said effective capacitance based on charging and discharging of said RC network from said drive current.

19. The computer readable medium as set forth in claim 14, wherein instructions for determining a new drive current for said circuit from said drive voltage and said effective capacitance comprises instructions for:

selecting an input signal slew rate for simulation of an input signal to said circuit; and

accessing said circuit characterization model to extract a drive current based on said drive voltage, effective capacitance, and said input signal slew rate selected.

20. The computer readable medium as set forth in claim 14, wherein:

said integrated circuit comprises at least one standard cell;

said circuit comprises a gate level circuit implemented on said standard cell; and

said RC network comprises an interconnect network on said integrated circuit for coupling said driving point to said receiving point.

21. The computer readable medium as set forth in claim 14, further comprising instructions for:

selecting, from one of said plurality of drive currents, a drive current with the largest value as a peak current; and

calculating peak power from said peak current.

22. A computer readable medium, comprising a plurality of instructions, which when executed by a computer, causes the computer to determine timing delays for a circuit in an integrated circuit, said instructions for:

determining a resistive-capacitive ("RC") network between a driving point and a receiving point, said circuit driving said RC network at said driving point;

selecting a plurality of time instances for analysis of said circuit;

determining a load capacitance for each of said time instances, said load capacitance specifying a capacitance from said driving point of said circuit;

determining operation of said circuit at a new time instance based on said load capacitance of a previous time instance; and

determining timing delay parameters based on operation of said circuit and response to said RC network at said time instances.

23. The computer readable medium as set forth in claim 22, wherein instructions for determining operation of said circuit at a new time instance based on said load capacitance of a previous time instance comprises instructions for:

selecting an initial drive current;

determining a drive voltage, corresponding to said drive current, by simulating the drive, at said driving point, of said RC network with said initial drive current;

determining a new drive current for said circuit from said drive voltage and said load capacitance; and

repeating the steps of determining a drive voltage from said load capacitance for said drive currents.

24. The computer readable medium as set forth in claim 22, wherein instructions for determining a new drive current for said circuit from said drive voltage and said load capacitance comprises instructions for:

storing a circuit characterization model for said circuit, said circuit characterization model depicting relationships among input signal slew rate, load capacitance, drive current and drive voltage for said circuit; and

selecting an input signal slew rate for simulation of an input signal to said circuit; and

accessing said circuit characterization model to extract a drive current based on said drive voltage, effective capacitance, and said input signal slew rate selected.

25. A computer implemented method for determining timing delay for a circuit in an integrated circuit, said method comprising the steps of:

determining a resistive-capacitive ("RC") network between a driving point and a receiving point, said circuit driving said RC network at said driving point;

storing a circuit characterization model for said circuit, said circuit characterization model depicting relationships among input signal slew rate, load capacitance, current at said driving point and voltage at said driving point for said circuit;

selecting a plurality of time instances;

selecting an initial drive current;

determining a drive voltage for each of said time instances, corresponding to said drive current, by simulating the drive, at said driving point, of said RC network with said initial drive current;

determining an effective capacitance for each of said time instances as a load for said circuit;

determining a new drive current for each of said time instances for said circuit from said drive voltage and said effective capacitance of a previous time instance;

repeating the steps of determining a drive voltage and determining an effective capacitance for said plurality of drive currents at each of said time instances;

determining a voltage at said receiving point from a transfer function of said RC network;

determining timing parameters for RC network propagation delay from said voltage at said driving point and said voltage at said receiving point;

receiving an input voltage to said circuit;

determining a voltage at said driving point from an impedance of said RC network and said driving currents; and

determining timing parameters for driving instance delay of said circuit from said input voltage to said voltage at said driving point.